

Are we spending our verification resources wisely?

Moderated by: Brian Bailey

Panelists: Joseph Rothman: ProDesign
Janick Bergeron: Synopsys
Ira Chayut: nVidia
Peter Becker: Software Prototype Technologies
Sunil Kakkar: Freescale

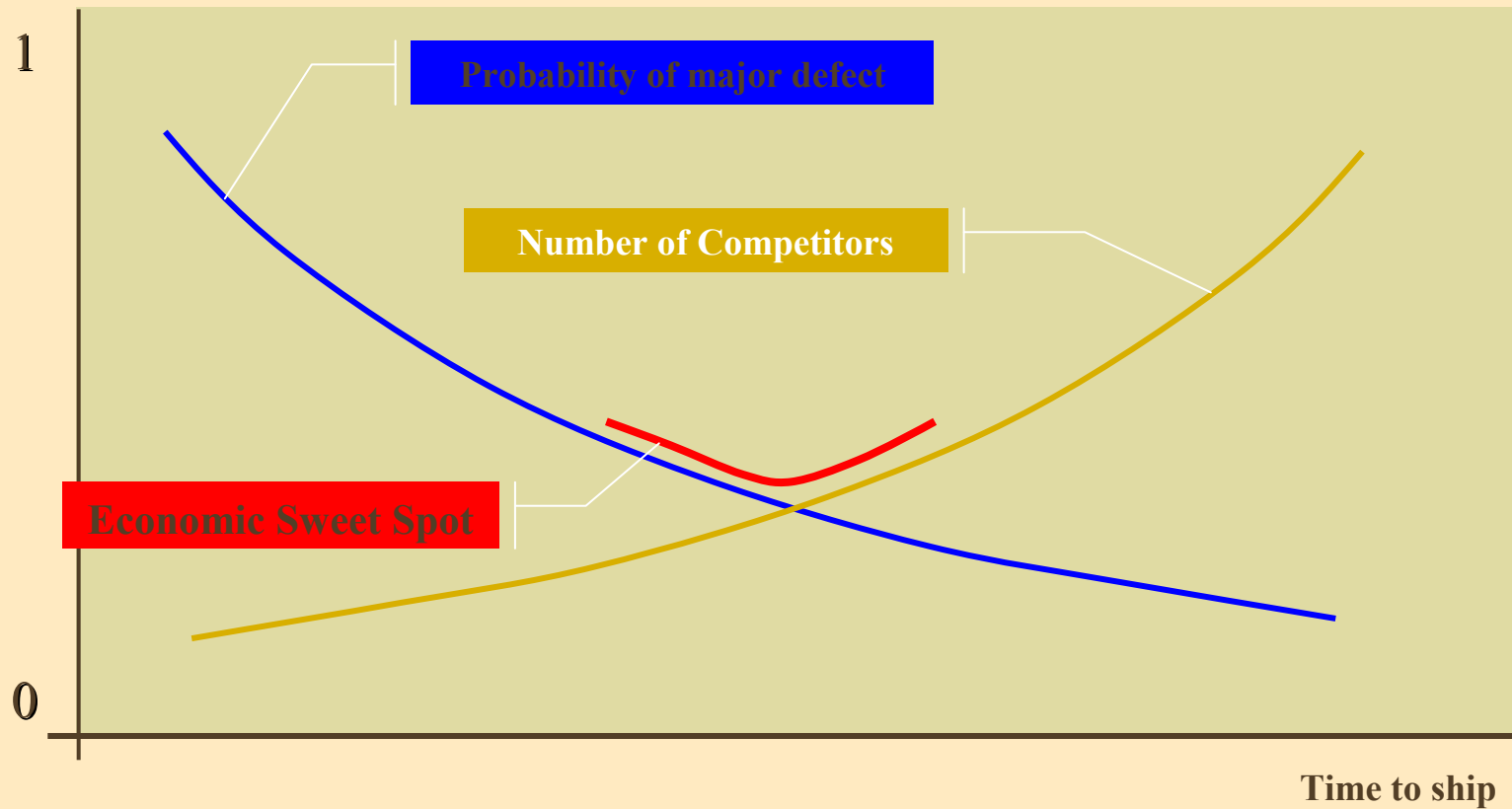
Organized by: Brian Bailey: Brian Bailey Consulting
Dave Whipp: nVidia

In previous episodes...

- **Value != Size != Complexity**
- **Complexity = (Implementation + $\sum ip$ + SW)**
 - * **degree of interaction**
 - * **tool degradation factor**
 - / abstraction**
- **Design != Implementation**
- **Release = Risk Management**

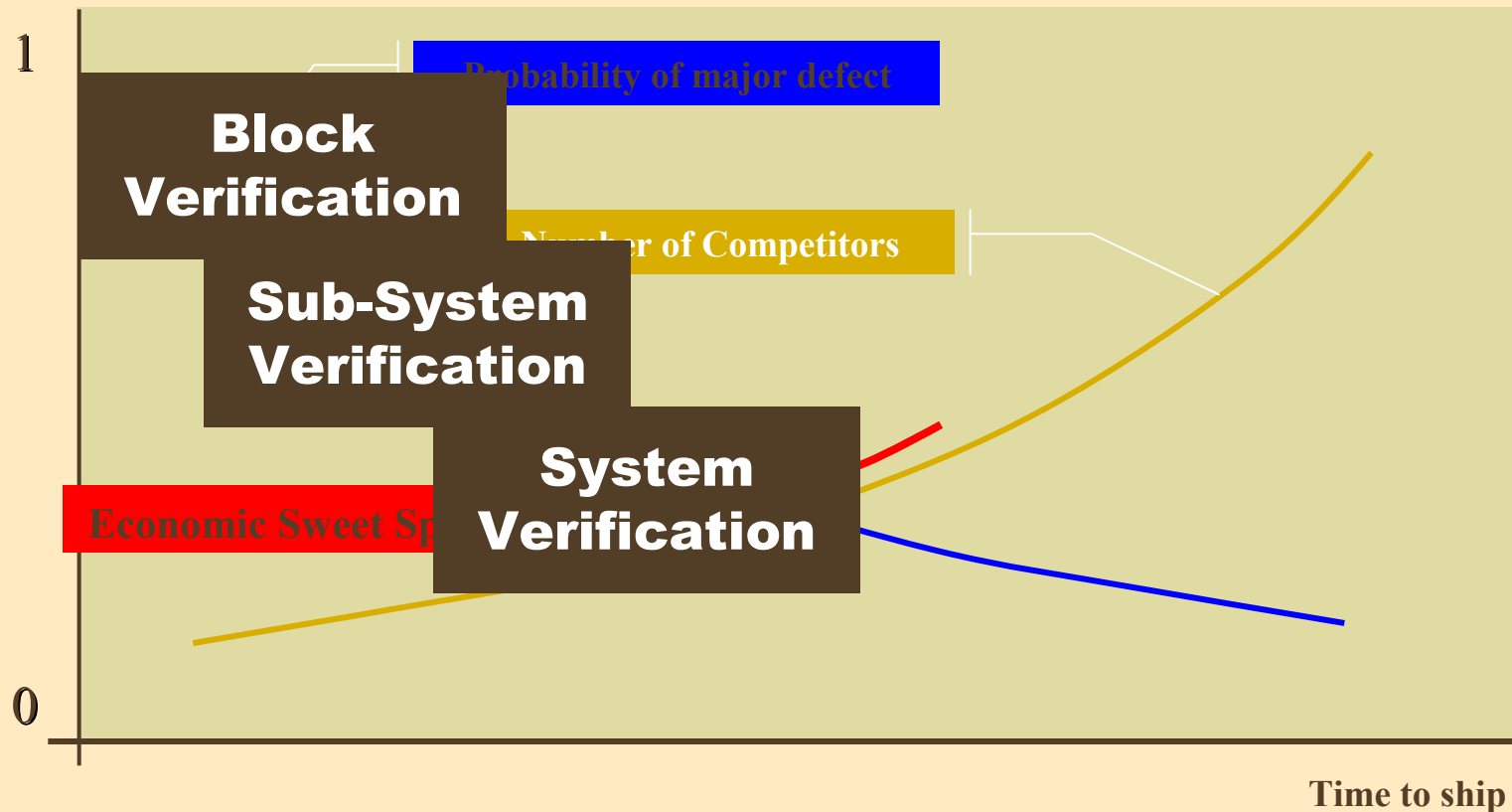
Reality and Economics

Probability



Reality and Economics

Probability



- #1 Important Verification Performed Late**
- #2 Tools based on an RTL flow**
- #3 Product differentiation by Software**

Panelists

Janick Bergeron

Ira Chayut

Joseph Rothman — Last minute substitute

Peter Becker

Sunil Kakkar

Moderated by Brian Bailey

Are We Spending Our Verification Resources Wisely?

Janick Bergeron
Synopsys Inc

February, 2005



Are we?

- Of course!
 - No one is foolish on purpose
 - Things work (sort of)
- But we know we have a problem
 - Clearly previously described

What is the problem?

- We are too happy about the status quo!

"Many of the heroes and redeemers we most admire were unhappy people who found it impossible to change how they felt about the world - which left them no choice but to change the world itself."

-- Daniel Gilbert

prof of Psychology, Harvard

author "*Stumbling on Happiness*"

Who benefits from the gap?

- Last great barrier to entry
 - Established companies rely on derivation
- New companies/products not verification challenges
 - Example: iPod
- If verification challenge is eliminated...
 - Race to the bottom!

Shouldn't this be "VerifCon"?

Janick Bergeron
Synopsys Inc

February, 2005





***N*VIDIA®**

**Are we spending our verification
resources wisely?**

Ira Chayut, Verification Architect

What Resources?

In increasing order of importance (IMHO):



- 1. Computer Farm Usage Time**
- 2. Simulation License Usage Time**
- 3. Engineer Time**
- 4. Time to Market**

Short Answer



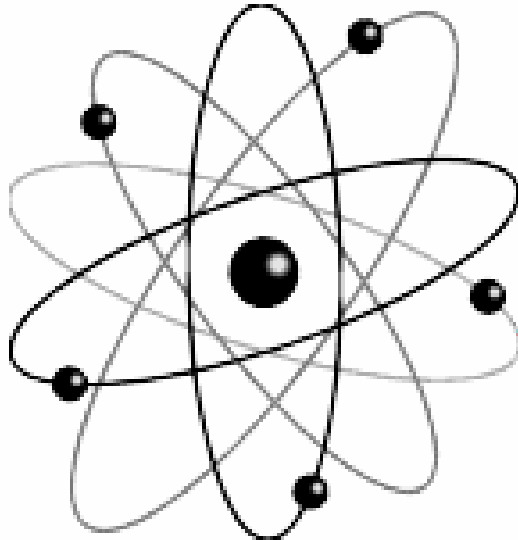
- **If your company is profitable and successful, then your processes are working – at least for the moment**
- **While you may be able to improve on your processes, you can also break them**

Long Answer



- **As chips get more complex**
 - simulation hosts also get faster – but not fast enough
 - burden of full-chip-level verification increases (geometrically?) faster
- **Simulators have also improved, but the (subjective) net result is that we are running in place at about 1 to 10 clocks/second**
- **the number of clock cycles needed going up super-linearly with chip complexity**

Can the Verification Effort be Reduced?



- **Most design engineer hours spent on unit-level designs**
☺ **scales with system complexity**
- **Most verification engineer (and simulation) hours spent on superunit and system-level verification**
☹ **does NOT scale with system complexity**
- **Can increased verification at the unit-level?**

Can the Verification Effort be Accelerated?

- Reduce simulation cycles with:

- High-end emulation
- Low-cost commercial emulation
- Home-brewed FPGA prototypes
- Formal and semi-formal tools
- Constraint-solving interactive testbenches



Soft HW Reduces Verification Burden?

Do programmable and configurable ASICs require less verification?



- No, as there are now more possible configurations and applications to verify
- Yes, as the “atomic” behaviors and interconnects can be more easily verified and the “software” doesn’t roadblock tape-out – application verification can overlap the back-end and fabrication flows

Summary

- **Chip complexity growth increasing verification costs**
- **Can try “divide and conquer” (focus more on unit test)**
- **Emulation or formal methods can reduce simulation**
- **Soft HW can push off verification cycles to real silicon**

Software Prototype Technologies

Peter Becker

CEO

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A View from the Software Side

- We thought you guys had all the answers!
- Misery loves company
- Problems remarkably similar; share solutions



What we have learned

- Without a hard-dollar business case, investing in verification improvements is very difficult.
- You can't test it all. Finding the right coverage metrics.



Building the Business Case

- 70% of development is test/rework
- Test and verification drives rework
 - Find all the defects
 - Find them as early as possible
- True verification enhancements reduce the rework.
- Sample metric: Project Cost/Rework Cost



The Case for Coverage

- You can't test everything
- Pick quantifiable metrics
 - Drives test design
 - Defines automation tools
- Improve the metrics
- Testing until the time, money or people run out is not a good coverage metric.



Some other thoughts

- Modularize the verification/test process
- Each deliverable in the process must be testable
- Let's collaborate



Thanks for your time

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Sunil Kakkar

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Where we need to improve

Use Coverage studies interactively
And keep in mind previous lessons learned

