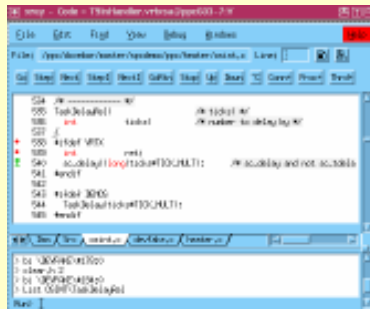




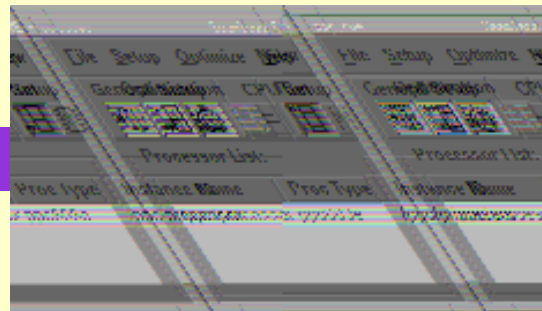
**SW Execution (Fast)**  
100,000 instructions/sec



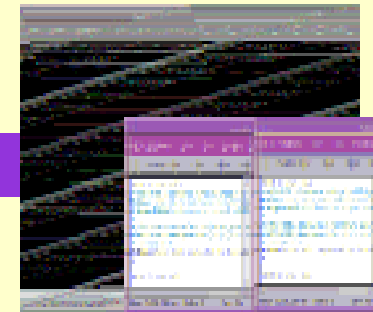
**Embedded Code**

**Fast  
Runtime**

*Seamless*  
Co-Verification Environment



**HW Simulation (Slow)**  
1 instruction/sec

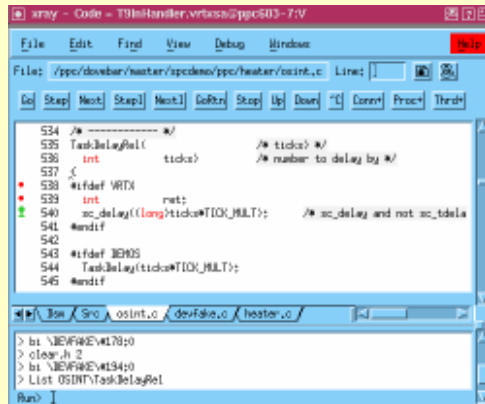


**Embedded Code**

**Comprehensive  
Verification**

# Seamless Delivers Both Coverage and Performance

SW Execution

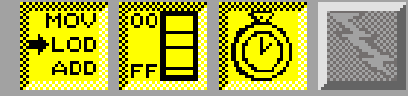


```

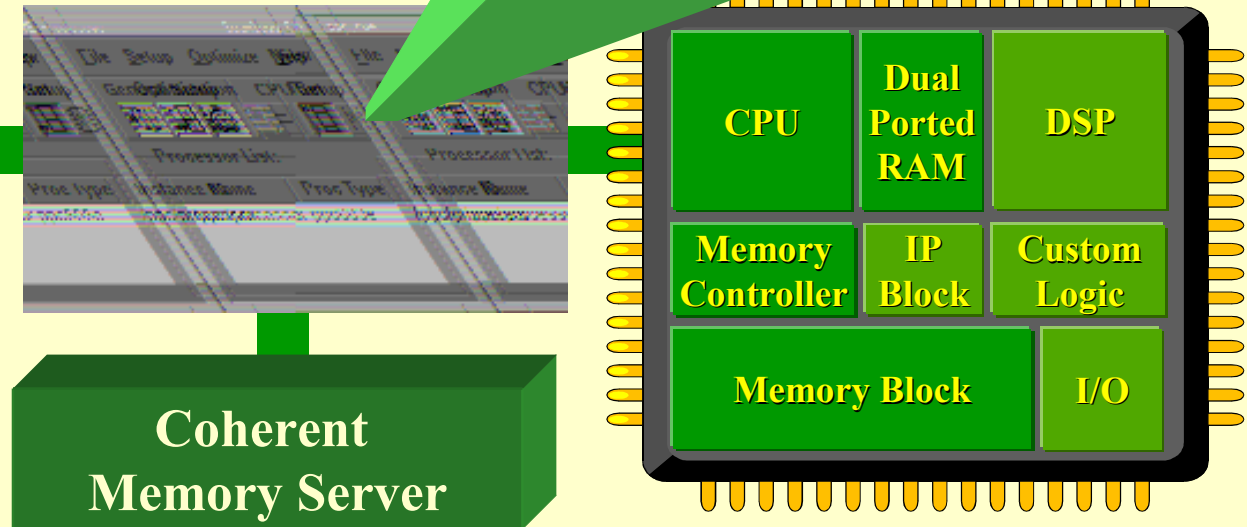
534 /* ----- */
535 TaskDelayRel( /* ticks: */
536             ticks) /* number to delay by */
537 {
538     #ifdef WDTX
539         int     ret;
540         ac_delay((long)ticks*TICK_MULT); /* ac_delay and not ac_delay
541     #endif
542
543     #ifdef BEHNS
544         TaskDelay(ticks*TICK_MULT);
545     #endif
    
```

*Seamless*  
Co-Verification Environment

Optimization



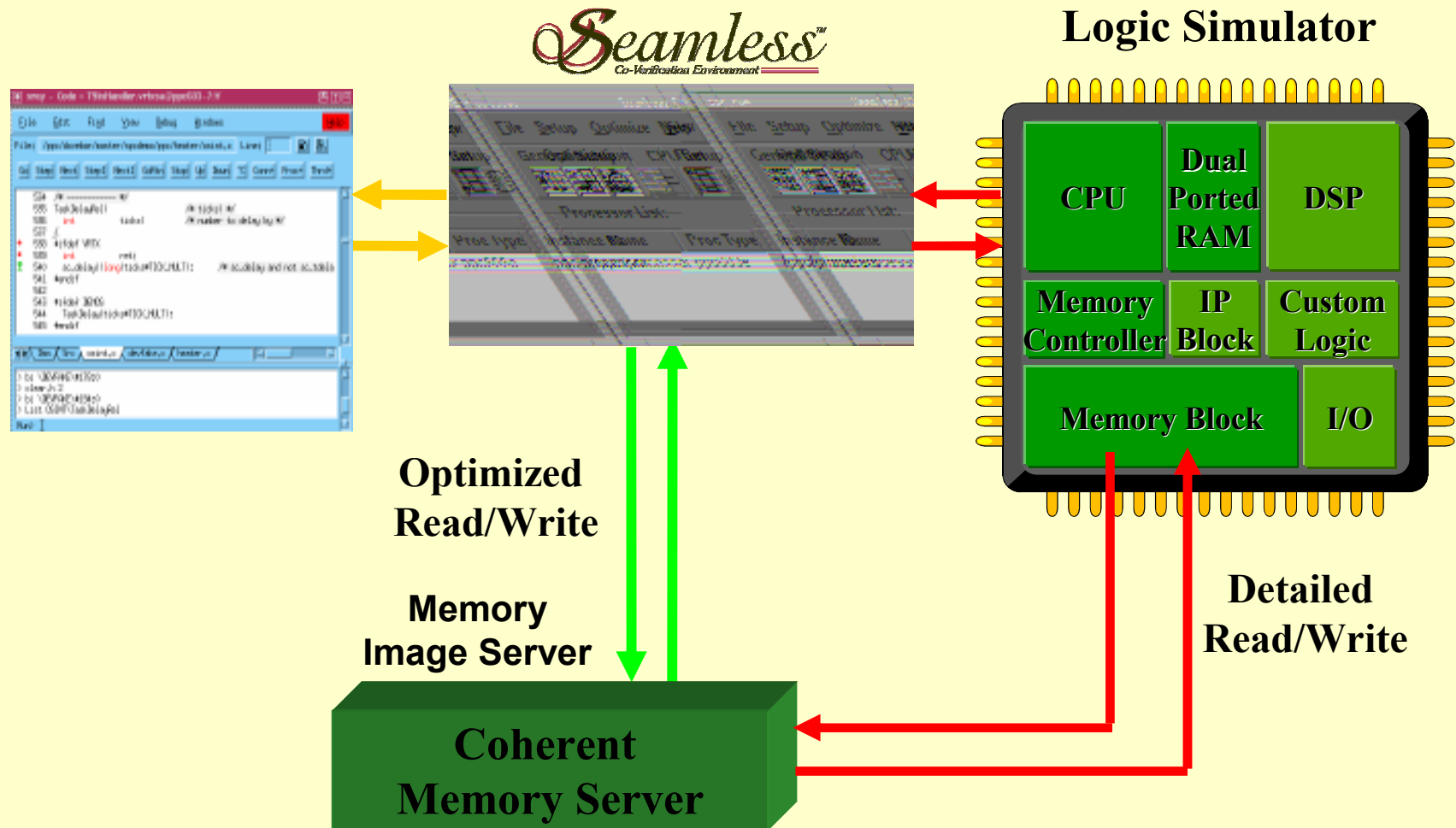
HW Simulation



Coherent  
Memory Server

- Fast run-time
  - Direct memory operations to the Coherent Memory Server

- Comprehensive verification
  - Boot and run code from the hardware



# Optimization are fully controlled by the user

